

39. (New) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, a gate electrode of said third transistor receiving a control signal; and

an eighth transistor inserted between said second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

REMARKS

The following remarks are fully and completely responsive to the Office Action dated September 12, 2002. Claims 1, 3-6, 8-20, 22-25 and 27-39 are pending in this application with claims 2, 7, 21 and 26 cancelled by the present Amendment. In the outstanding Office Action claims 2-5, 8, 11, 23, 27 and 30 were objected to; claims 11-13, 15, 30-32 and 34 were rejected under 35 U.S.C. § 112, second paragraph; claims 1-6, 9,

10 and 16 were rejected under 35 U.S.C. § 102(b); claims 11-15, 17, 18, 21-25 and 28-35 were rejected under 35 U.S.C. § 103(a) (two different rejections). Claims 7, 8, 19, 20, 26 and 27 were acknowledged as containing allowable subject matter. No new matter has been added. Claims 1, 3-6, 8-20, 22-25 and 27-39 are presented for consideration.

Claim Objections

Claims 2-5, 8, 11, 23, 27 and 30 were objected to for the formal matters identified in the Office Action dated September 12, 2002. Applicants' amendments to claims 1, 3, 4, 5, 8, 11, 23, 27 and 30 include the corrections suggested by the Examiner. Accordingly, Applicants respectfully request reconsideration and withdrawal of the objection to claims 3-5, 8, 11, 23, 27 and 30.

35 U.S.C. § 112, Second Paragraph

Claims 11-13, 15, 30-32 and 34 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Claims 11, 15, 30 and 34 have been amended such that claims 11-13, 15, 30-32 and 34 now particularly point out and distinctly claim the subject matter which Applicants regard as the invention. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 11-13, 15, 30-32 and 34 under 35 U.S.C. § 112, second paragraph.

35 U.S.C. § 102(b)

Claims 1-6, 9, 10 and 16 were rejected under 35 U.S.C. § 102(b) as being anticipated by Branson (U.S. Patent No. 5,508,644). This rejection has been rendered moot by the amendment of claim 1 to include the limitations of claims 2 and 7. In the Office Action dated September 12, 2002, the Examiner indicated that claim 7 contained allowable subject matter. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) of claim 1 and of claims 3-6, 9, 10 and 16 which depend directly or indirectly from claim 1.

35 U.S.C. § 103(a)

Claims 11-15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art (Figures 1-7) in view of Branson (U.S. Patent No. 5,508,644). This rejection has been rendered moot by the amendment of claim 1, from which claims 11-15 either directly or indirectly depend, to include the limitations of claims 2 and 7. The Office Action indicated that claim 7 contained allowable subject matter. Thus, claims 11-15 now depend from a claim that contains allowable subject matter. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 11-15 under 35 U.S.C. § 103(a).

Claims 17, 18, 21-25 and 28-35 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' admitted prior art (Figures 1-7) in view of Branson (U.S. Patent No. 5,508,644) and Oklobdzija (U.S. Patent No. 6,232,810 B1). This rejection has been rendered moot by the amendment of claim 17 to include the limitations of claims 21 and 26. The Office Action indicated that claim 26 contained allowable subject matter.

Therefore, claims 17, 18, 22-25 and 28-35 contain allowable subject matter. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 17, 18, 22-25 and 28-35 under 35 U.S.C. § 103(a).

New Claims

Applicants have added new claims 36-39.

Claim 36 corresponds to the combination of claims 17, 18 and 19. The Office Action indicated that claim 19 contained allowable subject matter and thus claim 36 should also be allowable.

Claim 37 corresponds to claim 20 and depends from claim 36. Claim 20 should be allowable since the Office Action indicated that the combination of claims 17, 18 and 19 would be allowable and because the Office Action indicated that claim 20 would be allowable if it depended from an allowable claim.

Claim 38 corresponds to the combination of claims 1, 2 and 15, and claim 39 corresponds to the combination of claims 17, 21 and 34. These claims are patentable for the reasons discussed below.

Claim 38 recites a differential amplifier circuit comprising a latch unit and a differential input portion. The differential input portion includes a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode. The control electrodes of the first and second transistors are supplied with a differential input signal. A third transistor for keeping a minute current flowing through the first and second transistors is inserted between a first power line and a common node to which the first electrodes of the first and second transistors are connected. A gate electrode of the

third transistor receives a control signal. An eighth transistor is inserted between the second power line and the common node to which the first electrodes of the first and second transistors are connected. The control electrode of the eighth transistor is supplied with a fourth control signal.

Claim 39 recites a semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal. A latch circuit latches an output signal of the differential amplifier circuit. A clock source generates a clock and supplies the generated clock to the differential amplifier circuit. The differential amplifier circuit includes a latch unit and a differential input portion. The differential input portion includes a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode. The control electrodes of the first and second transistors are supplied with the differential input signal. A third transistor, for keeping minute current flowing through the first and second transistors, is inserted between a first power line and a common node to which the first electrodes of the first and second transistors are connected. A gate electrode of the third transistor receives a control signal. An eighth transistor is inserted between the second power line and the common node to which the first electrodes of the first and second transistors are connected, the control electrode of the eighth transistor being supplied with a fourth control signal.

Both claims 38 and 39 require that the gate electrode of the third transistor receives a control signal.

The Office Action, with respect to claim 21, asserted that transistor 26 shown in Figure 1 of Branson was the third transistor recited in Applicants' claims. The gate electrode of transistor 26, however, is connected directly to voltage V_{DD} . Accordingly,

transistor 26 does not receive a control signal. Therefore, the combination of Applicants' admitted prior art, Branson and Oklobdzija fails to teach and/or suggest a third transistor for keeping a minute current flowing through the first and second transistors that is inserted between a first power line and a common node to which the first electrodes of the first and second transistors are connected, a gate electrode of said third transistor receiving a control signal. Therefore, claims 38 and 39 recite subject matter which is neither disclosed nor suggested by any combination of the prior art. Accordingly, Applicants respectfully request consideration and allowance of claims 38 and 39.

Conclusion

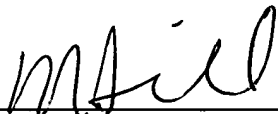
Applicants' amendments and remarks have overcome the objections and rejections set forth in the Office Action dated September 12, 2002. Specifically, Applicants' amendments have overcome the objections to claims 2-5, 8, 11, 23, 27 and 30 and the rejection of claims 11-13, 15, 30-32 and 34 under 35 U.S.C. § 112, second paragraph. Applicants' remarks have distinguished claims 1, 3-6, 9, 10 and 16 from Branson and thus overcome the rejection of these claims under 35 U.S.C. § 102(b). Applicants' remarks have also distinguished claims 11-15 from Branson and thus overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants' remarks have also distinguished claims 17, 18, 22-25 and 28-35 from the combination of Applicants' admitted prior art, Branson and Oklobdzija, and thus, overcome the rejection of these claims under 35 U.S.C. § 103(a). Applicants have added new claims 36-39 which are allowable for the reasons discussed above. Accordingly, claims 1, 3-6, 8-20, 22-25 and 27-39 are in condition for

allowance. Accordingly, Applicants respectfully request consideration and allowance of claims 1, 3-6, 8-20, 22-25 and 27-39.

Applicants submit that the application is now in condition for allowance. If the Examiner believes that the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 100021-00069.

Respectfully submitted,



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Enclosures: Petition for Extension of Time
Marked-Up Copy of Amended Claims
Amendment and Fee Transmittal

MARKED-UP COPY OF AMENDED CLAIMS

1. (Amended) A differential amplifier circuit comprising a latch unit and a differential input portion, wherein [a minute current is kept to flow through said differential input portion];

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal; and

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit.

3. (Amended) The differential amplifier circuit as claimed in claim [2] 1, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of said differential amplifier circuit.

4. (Amended) The differential amplifier circuit as claimed in claim [2] 1, wherein the differential input portion further comprises:

a fourth transistor for supplying a drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; [and] wherein

said third transistor is connected in parallel to said fourth transistor.

5. (Amended) The differential amplifier circuit as claimed in claim 4, wherein the control electrode of said third transistor is supplied with a first control signal for constantly supplying [a] the minute current during the operation of said differential amplifier.

8. (Amended) The differential amplifier circuit as claimed in claim [7] 1, wherein [the] a first control signal supplied to the control electrode of said third transistor is set to a level for supplying a predetermined drive current at the time of signal determination in said differential amplifier circuit, while causing [a] the minute current to flow through said first and second transistors at other than the time of signal determination during the operation of said differential amplifier.

11. (Amended) The differential amplifier circuit as claimed in claim 1, further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second [electrode] transistor for shorting the second electrodes of said first and second transistors in accordance with a second control signal.

15. (Amended) The differential amplifier circuit as claimed in claim 1, further comprising:

an eighth transistor inserted between [said] a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

17. (Amended) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an

output signal of said differential amplifier circuit, and a clock source generating a clock and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein [a minute current is kept to flow through said differential input portion];

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal; and

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit.

22. (Amended) The semiconductor integrated circuit device as claimed in claim [21] 17, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of said differential amplifier circuit.

23. (Amended) The semiconductor integrated circuit device as claimed in claim [21] 17, wherein the differential input portion further comprises:

a fourth transistor for supplying a drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; [and] wherein

said third transistor is connected in parallel to said fourth transistor.

27. (Amended) The semiconductor integrated circuit device as claimed in claim [26] 17, wherein [the] a first control signal supplied to the control electrode of said third transistor is set to a level for supplying a predetermined drive current at the time of signal determination in said differential amplifier circuit, while causing [a] the minute current to flow through said first and second transistors at other than the time of signal determination during the operation of said differential amplifier.

30. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second [electrode] transistor for shorting the second electrodes of said first and second transistors in accordance with a second control signal.

34. (Amended) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

an eighth transistor inserted between [said] a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

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